A 600×600 Pixel, 500 fps CMOS Image Sensor with a 4.4μm Pinned Photodiode 5-Transistor Global Shutter Pixel

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Abstract

To realize a low cost image sensor, while maintaining a 500 fps-class high frame rate, we have developed a prototype image sensor where a 600×600 imaging array with a 4.4μm global shutter pixel and multiple pipeline analog-to-digital converters (ADCs) are implemented. In this paper, its image sensor architecture, pixel configuration and operation are described and characterization results are reported.

I. Introduction

Machine vision and high frame rate applications usually require the global shutter operation to "freeze" the image. In global shutter pixels, an in-pixel signal memory, an additional global reset gate and a global transfer gate should be equipped, which results in a larger pixel size than that of general purpose CMOS imagers. In previously reported high speed CMOS image sensors with the global shutter functionality, relatively large pixels, ranging from 7μm to 16 μm, have been used [1-3]. However, the large pixel size results in a large die size and thus high image sensor cost. Therefore, pixel size reduction has been strongly requested for low cost applications and/or small module applications.

In this paper we present a 600×600 pixel prototype imager with a 4.4μm pitch 5-transistor global shutter pixel. The imager can operates at a high frame rate of 500fps.

II. Sensor Design

a. Chip specifications and structure

Figure 1 shows a block diagram of the image sensor. The pixel signals from a 600×600 imaging array are read out through top and bottom circuit blocks and transferred to analog signal chain / analog-to-digital converter (ASC/ADC) blocks. The column block consists of column gain amplifiers, sample-and-hold capacitors and a column decoder with column select switches.

The ASC/ADC block consists of second gain amplifiers and 8bit low power pipeline ADCs. A DAC/Buffer block contains bias generators and reference voltage generators that are controlled by two-wire serial I/F, thus yielding a fully digital interface. All internal pulses are generated by an internal timing generator (TG) so that external control/trigger inputs are minimized.

The chip handles pixel readout and signal processing at 200Mpixel/s with a 50MHz master clock and operates at 500fps with 600×600 full pixel resolution.

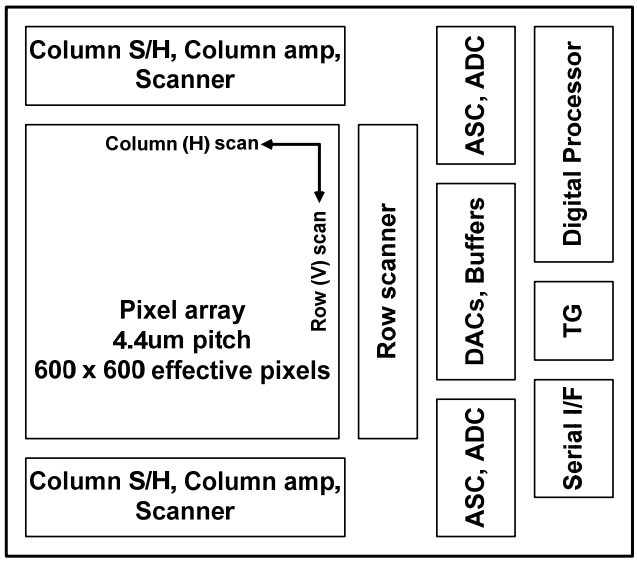

Figure 1. Block diagram of the chip.

b. Pixel configuration

The pixel consists of a pinned photodiode (PD), pixel memory (storage node M) and five transistors for pixel reset and readout as shown in Figure 2. The AB gate controls reset of the photodiode. This reset is global, i.e., all the pixels are reset simultaneously. The TX gate controls the charge transfer from PD to M. The complete charge transfer is required for both AB and TX operations to eliminate image lag and pixel-wise FPN.

In a global shutter mode, signal charge is transferred to node M, then the charge is read out in a similar manner to that of the conventional 3T pixel operation. Since a signal charge integration part and a readout part are separated by TX, the pixel allows simultaneous operations of charge integration and signal readout.

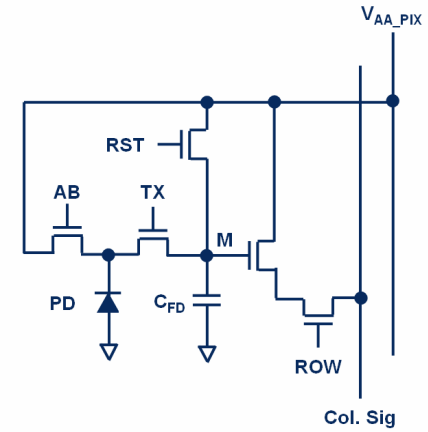

Figure 2. 5T global shutter pixel configuration

c. Signal chain

A schematic diagram of the signal chain is shown in Figure 3. The imager has two gain stages; one is in the column block and another in the video ASC block, as a primary gain stage and a secondary supplemental gain stage, respectively.

Pixel signal is amplified up to 8x by the column amplifier simultaneously to the pixel readout then stored on SH capacitors. Through a column select switch addressed by the column address decoder, stored signal in the SH capacitor is serially transferred to the ASC block followed by a low power 8bit ADC. Four ADC's, each operates at 50Msps, are integrated. Thus a total data rate reaches 200Msps.

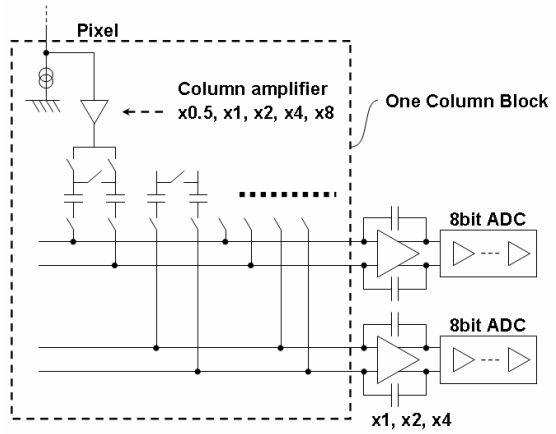

Figure 3. Signal chain of one column block

d. Global control and internal operation

A timing diagram for a frame operation is shown in Fig. 4. The sensor receives three external control pulses, 'START_EXPOSURE', 'END_EXPOSURE', and 'READ_START', each triggering the start of the exposure, the end of the exposure and the signal readout sequence. When 'START_EXPOSURE' is asserted, all photodiodes are reset by the global AB pulse that sweeps the charge out of the photodiode. Next, 'END_EXPOSURE' determines time for global TX that forces the charge to transfer from a photodiode to a memory node M. Readout of the charge in the memory node M starts when 'READ_START' pulse is asserted.

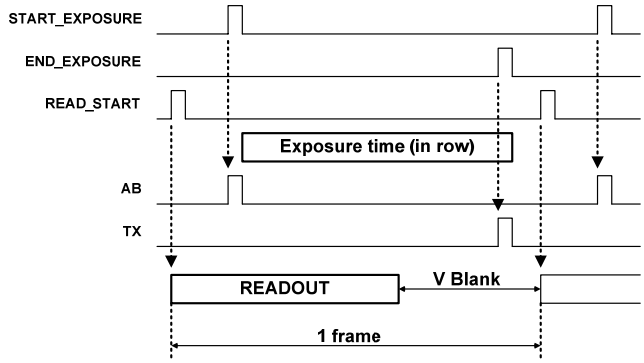

Figure 4. Operation timing

I2C interface is used for detail imager control. Also, two register banks are implemented, thus enabling instantaneous switching between two registered operation modes. This functionality helps enhance usability of high-speed imaging. For example, one register is set for a high-frame rate operation with reduced number of readout rows, and the other is set for reading out full resolution images. In this case, when an object is detected while the imager is operating in the high-frame rate mode, the system requests the imager to capture an full resolution image, thereby the imager immediately changes its operation mode for the full resolution snapshot readout. When the snapshot mode is chosen, the signal memory M should be reset to clean up noise charge or lag charge on the node during the charge integration period before the global TX is asserted.

III. Fabrication and Characterization

a. Fabrication

The 600×600 pixel image sensor was fabricated in 0.13μm 2P4M CMOS image sensor process. The prototype is a monochrome sensor with an on-chip

microlens array.

Figure 5 shows the top layout of the imager. An imager core including a pixel array and the rest of the analog blocks, together with integrated logic circuits, are implemented for prototyping. Video output is read out through 8bit × 4 parallel output ports, each handling a 50MHz data rate. Thus, a total output data rate of 200Mpix/sec is achieved. Imager core size is approximately 4.0mm × 4.0mm.

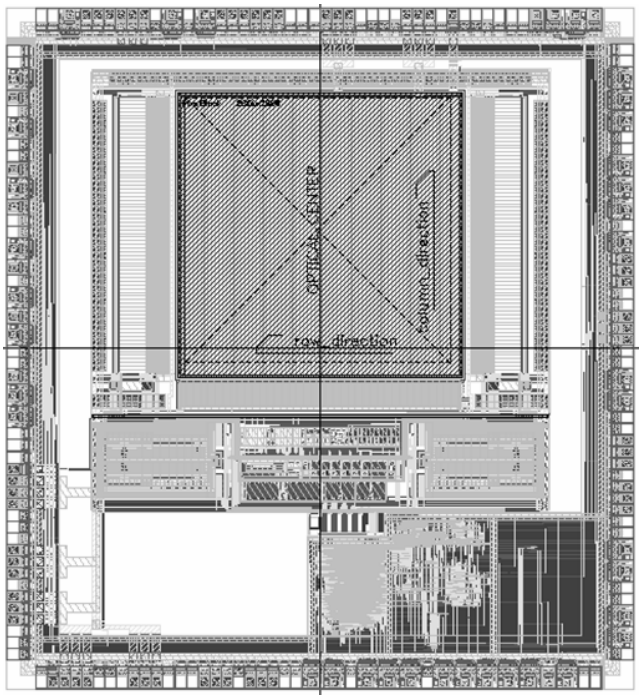

Figure 5 Prototype chip layout

b. Operation sequence for characterization

Besides the external trigger mode, the imager operation can be programmed with combinations of two registered modes. To perform characterization, we use a following operation sequence as shown in Figure 6; One cycle includes 8 fast readout frames and 8 full resolution readout frames. 32 effective rows are read out at 5000fps in the fast readout period then full resolution readouts at 500fps follow.

A full resolution image is evaluated from the first full resolution image. Also, image lag can be characterized with consecutive 8 frames in the full resolution readout period. Characterization was done under the 500fps full resolution condition.

c. Characterization results

Fig. 7 shows a spectral response. With an on-chip microlens, peak quantum efficiency reaches 63% at 500nm. Also the result shows good sensitivity against a wide wavelength range from near ultraviolet to near infrared. Quantum efficiency exceeds 20% within a range from 380nm to 830nm.

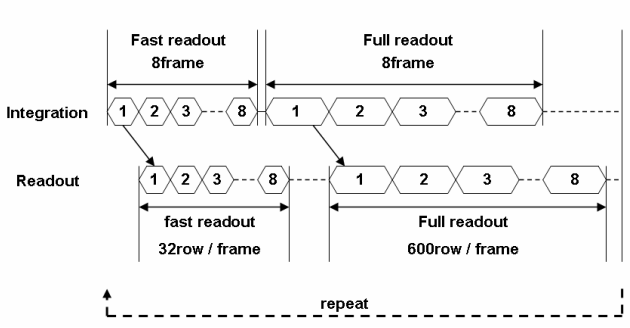

Figure 6. Operation cycle for characterization

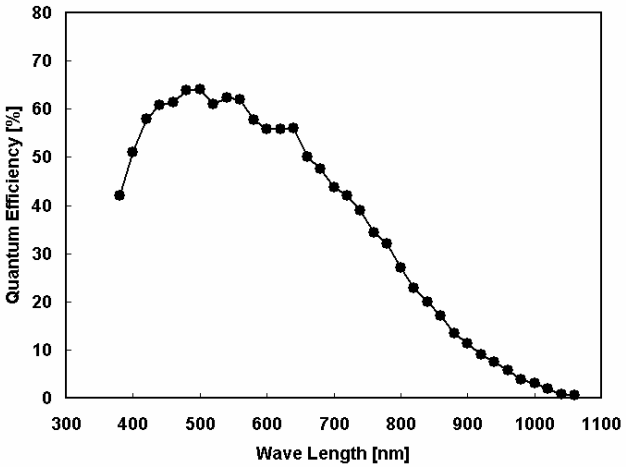

Figure 7. Spectral response

Image lag was negligibly small, which demonstrates the signal charge transfer from the pinned photodiode to both the memory node and the AB drain is almost complete.

Noise performance versus analog gain is plotted in Figure 8 with pixel-wise noise, temporal noise and structural noise. The data was obtained from one output port of 4, therefore offset variation between output ports are ignored. Total noise is very close to pixel random temporal noise and the result suggests main noise source is the pixel temporal noise that is caused by a reset operation of a floating node M in Figure 2. Capacitance of the floating node is estimated to be 3.4fF and it causes noise of 27 electrons-rms per reset operation. FPN including structural noise is smaller than 1/5 the pixel temporal noise when gain is larger than 2 and it is mostly invisible.

On the other hand, offset variation between signal chains was measured to be approximately 1.2LSBs at 4x gain, which corresponds to 17 electrons-rms. Although this noise level is smaller than 1/2 the total

noise at 4x gain, we can reduce the noise by offset adjustment in the backend process.
An image obtained from a snapshot and summary of imager specifications are shown in Figure 9 and Table 1, respectively.

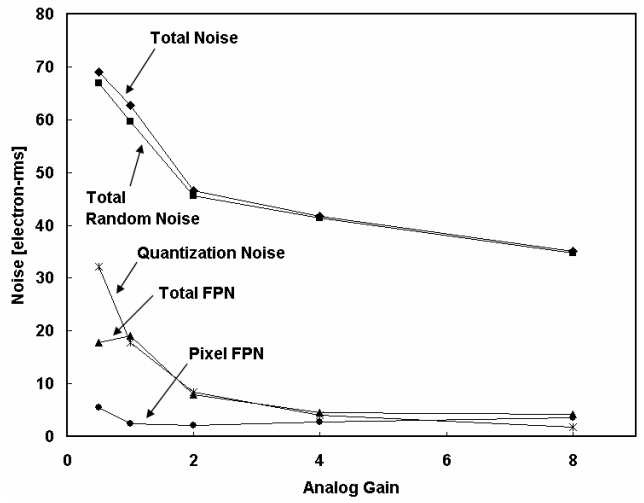

Figure 8. Noise measurement result

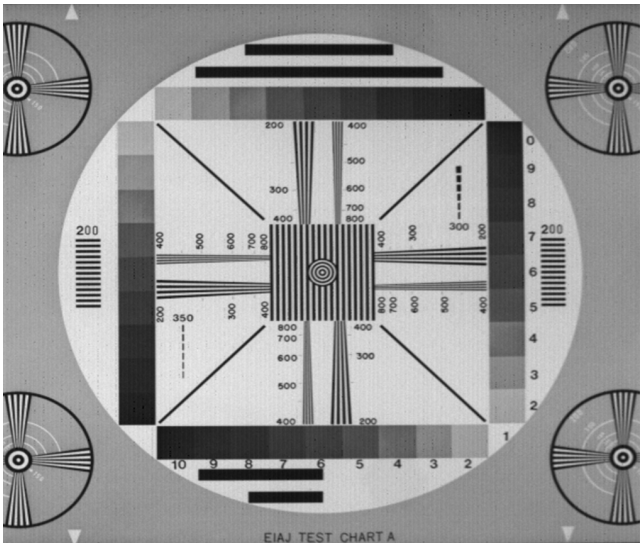

Figure 9. An output image from the first frame in a full resolution readout period in Figure 6 operating at 500fps. No correction of channel offset variations.

Table I. Specifications and Performance

Resolution	600 x 600
Pixel size	4.4 μm
Optical format	1/5 inch
Shutter scheme	Global shutter
Master clock	50 MHz
ADC resolution	8 bit
Full resolution frame rate	500 fps
Power consumption	248 mW
Peak quantum efficiency	63% at 500nm
Total noise	42 electrons at 4x gain
Linear full well capacity	12k electrons

IV. Conclusion

We have developed a prototype 600×600 pixel, 500 fps CMOS image sensor with a 4.4μm 5T pinned PD global shutter pixel for low-cost, high-frame rate imaging applications. It features a quick operation mode switching (ex. from a 5000fps windowing mode to a 500fps full resolution mode, and vice versa), while no degradation in image quality of the first frame after the switching is observed. High quantum efficiency of 63% at 500nm is obtained. The kTC noise associated with the in-pixel memory reset is a dominant noise source. Both FPN and image lag are reasonably suppressed.

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